

Fig. 5

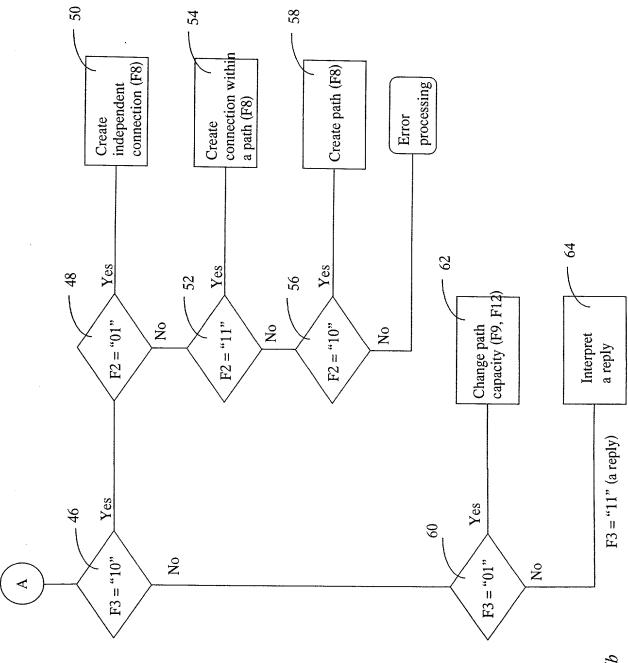
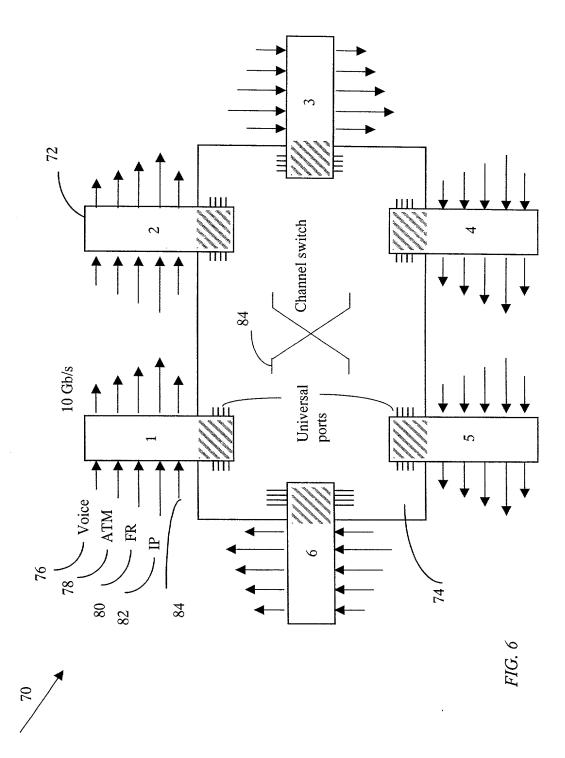
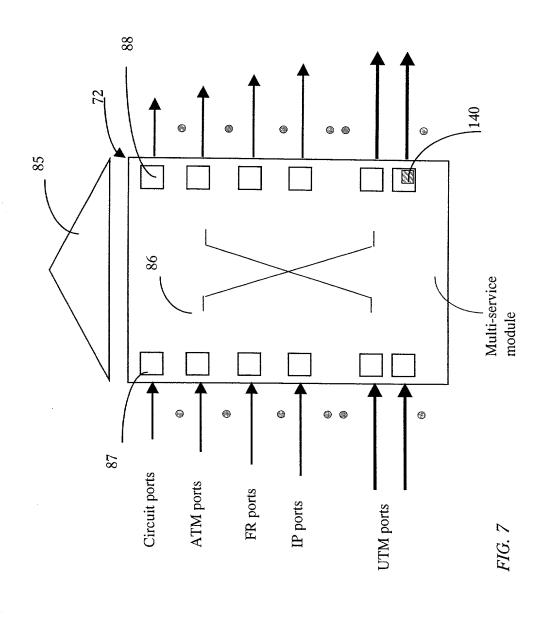


Fig. 5b





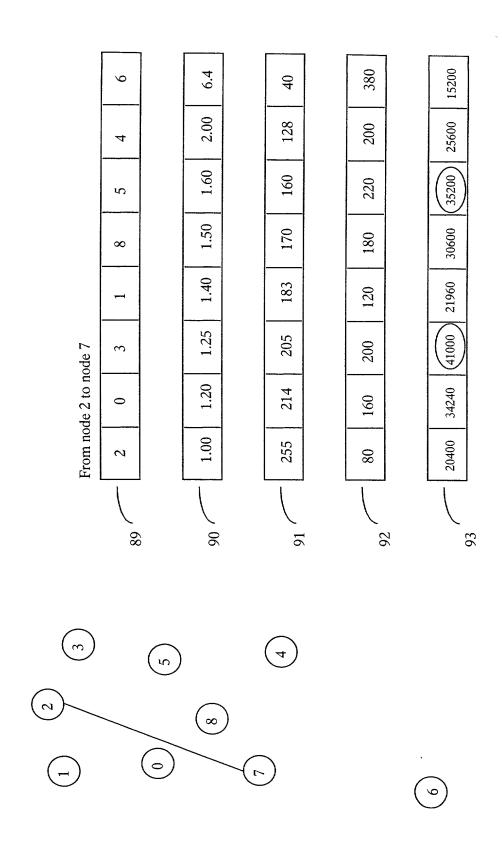
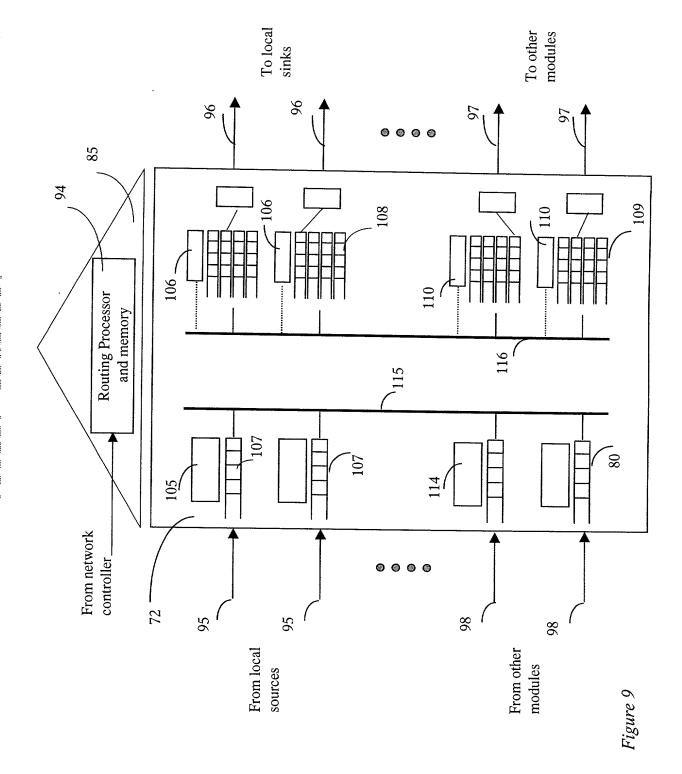


FIG. 8



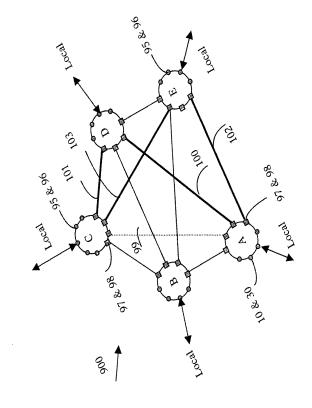
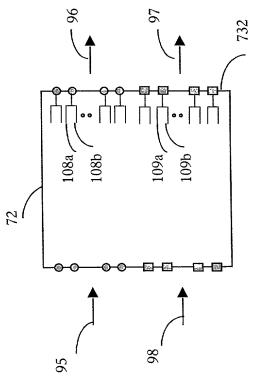


Figure 10



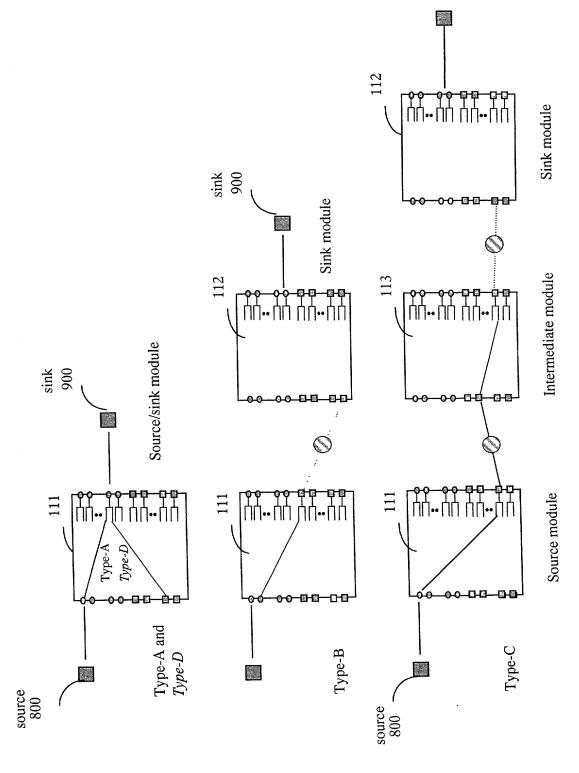


Figure 12

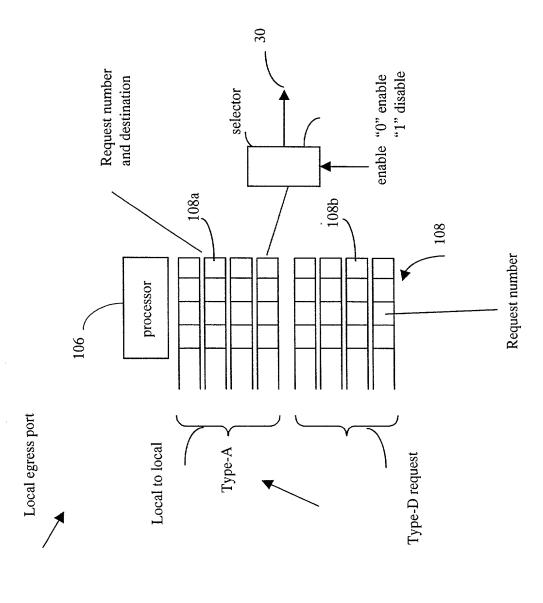


Figure 13

Core egress port

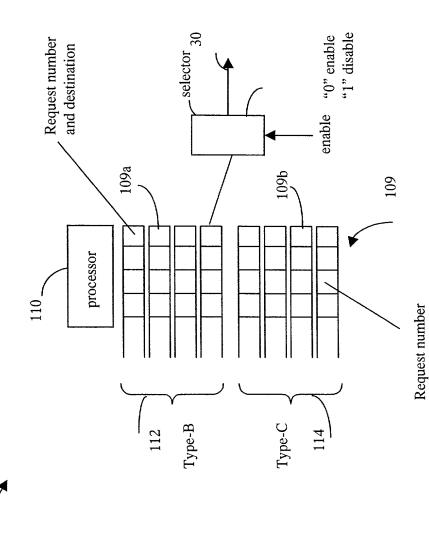


Figure 14

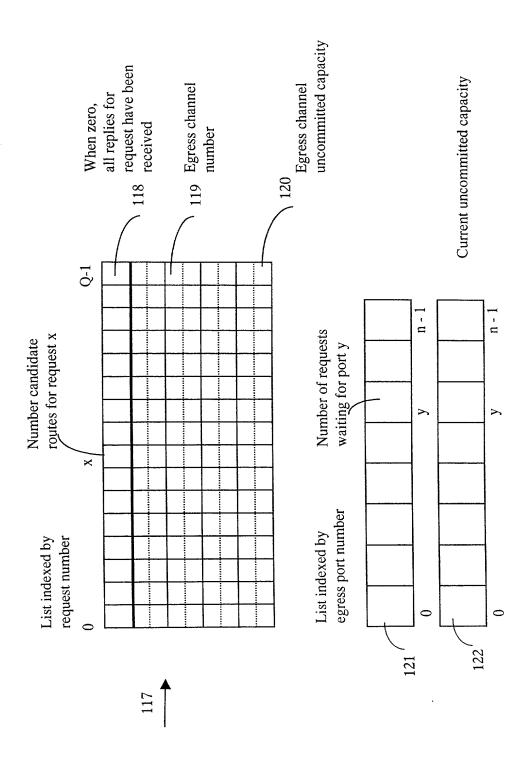


Figure 15

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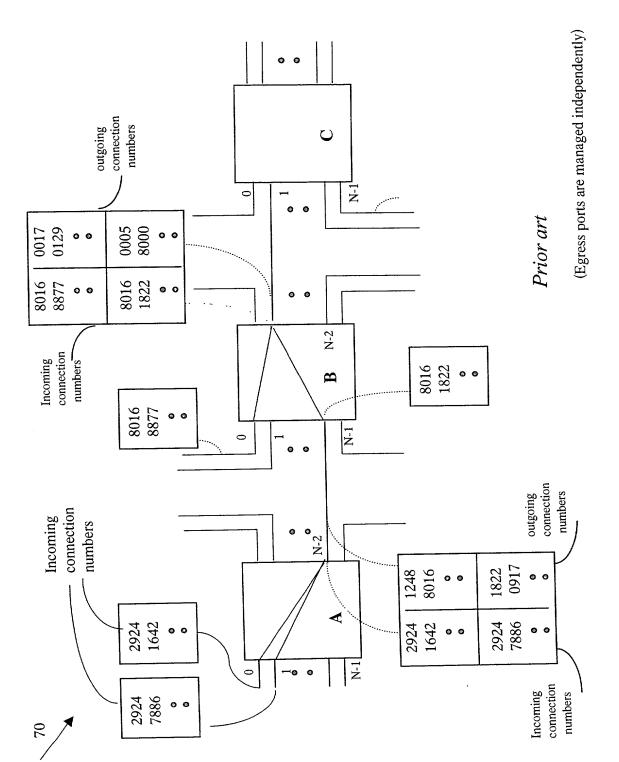
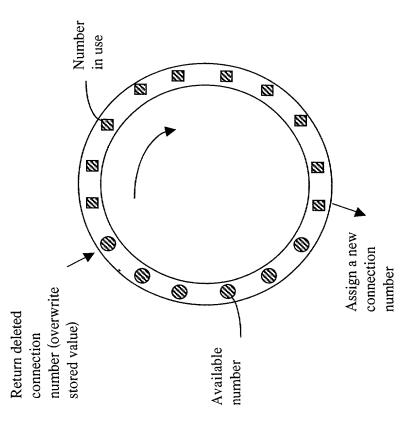


FIG. 17



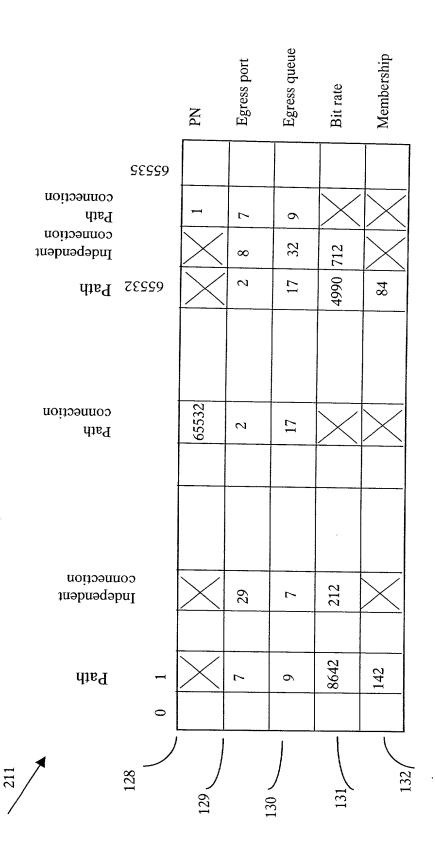


FIG. 15

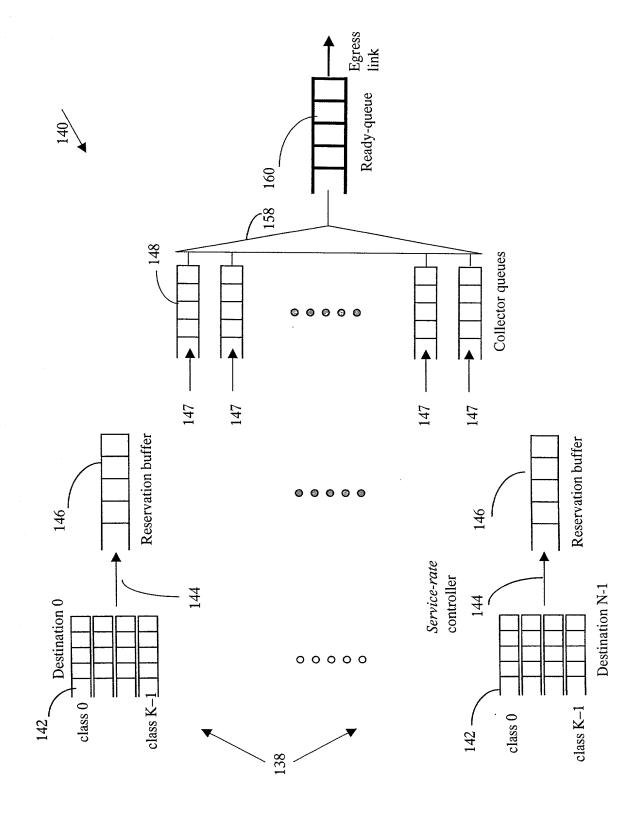


FIG. 20

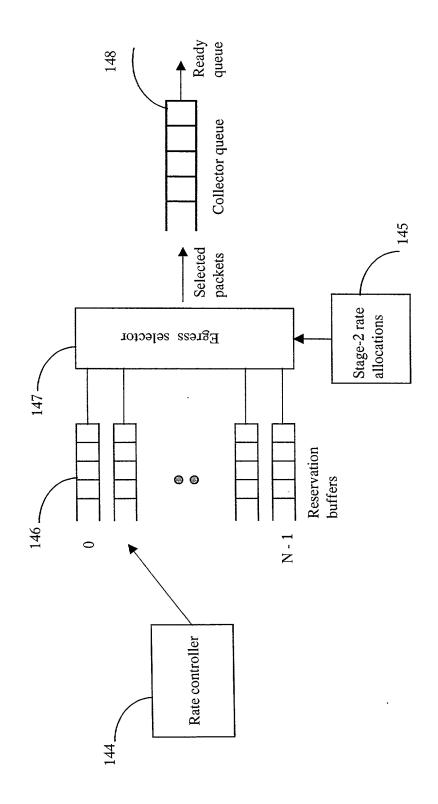


FIG. 21

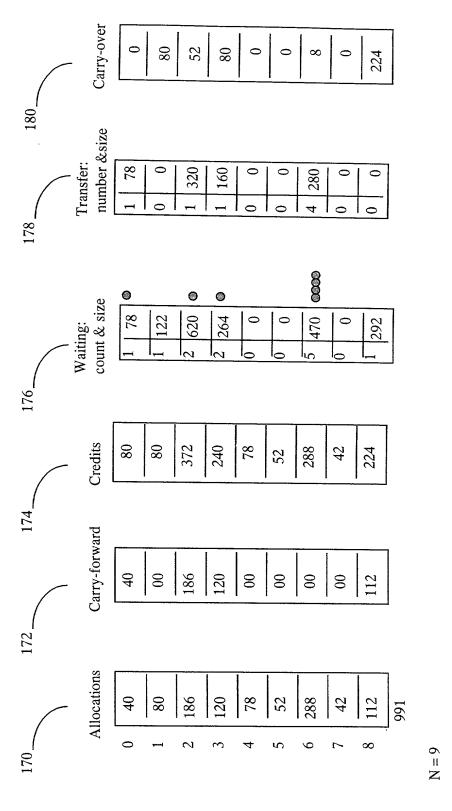
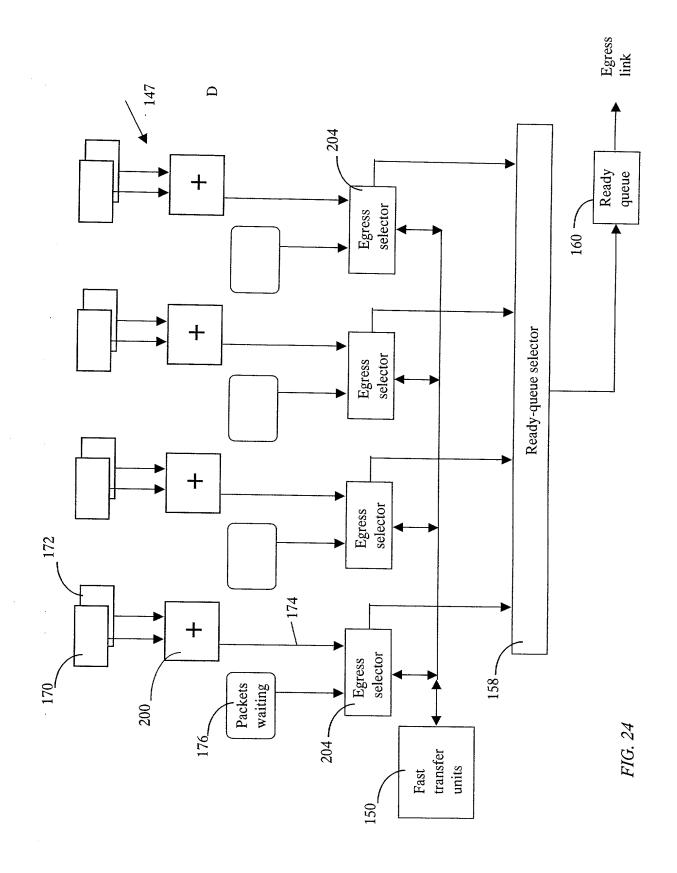


FIG. 22

(Arrivals during cycle: one packet of 100 bytes - stream 1 and one packet of 204 bytes - stream 6)

FIG. 23



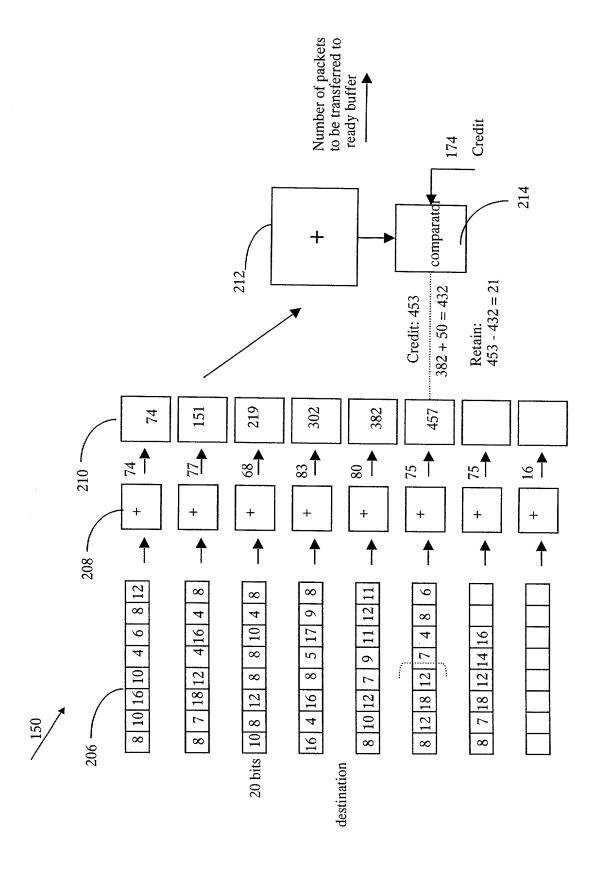


FIG. 25

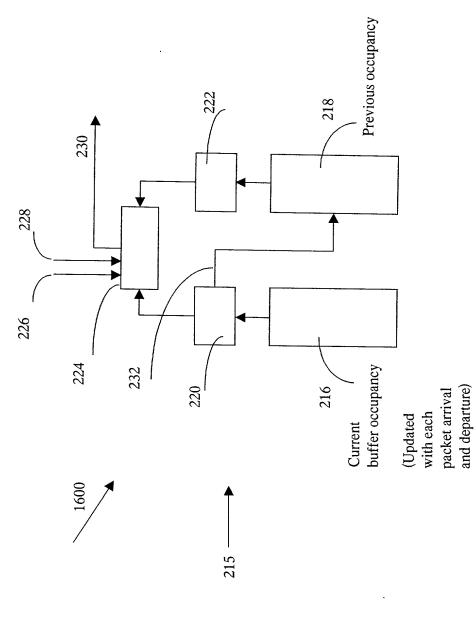


FIG. 2

1400	/	1
,		

Stream	Ositive	Ψ+	0	0
Str	Sosit	•		
tream buf	Positive or zero	+Δ1	. 0	0
fer oc	ero			
Stream buffer occupancy change	Negative	0	0	

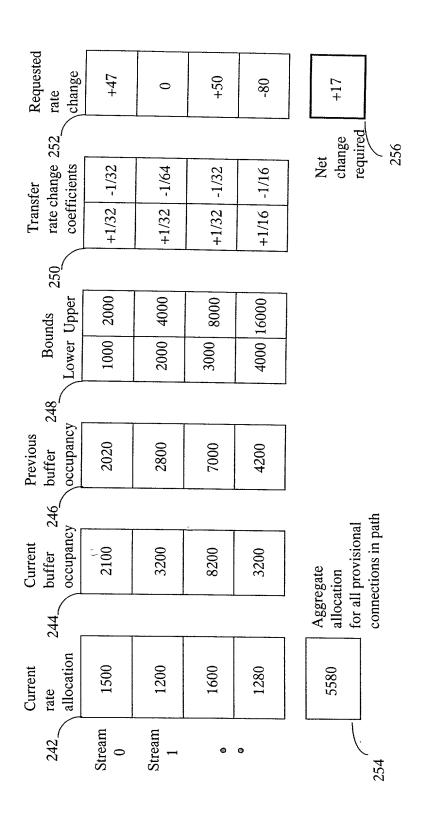


FIG. 28